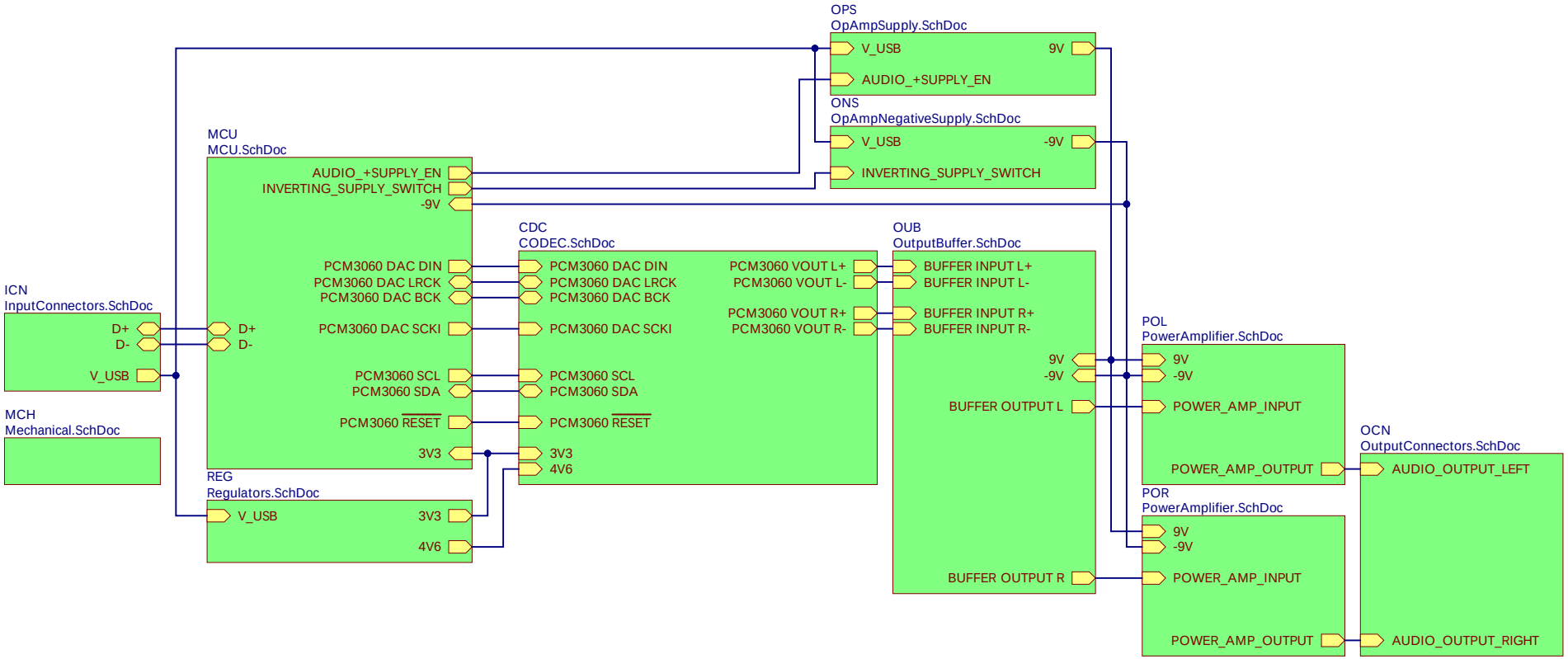

Title: Gould.SchDoc			Ploopy Corporation
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There's not really a good recommendation for what t o do with the ADC inputs if you're not going to use them. The safest bet is probably to have a low-impedance source driving them to VCOM, but this costs money and is therefore stupid if there's a more efficient solutio n available.

The abs. max range for these inputs is -0.3V to VCCish, so we could ground them without damaging the device. The ADC *should* read as the minimum possible value in this case, but since we never use it, that should be a moot point. And the signal won't wiggle, so that's probably good, too.

The ADC on the PCM3060 is not used in this application, so it is silly to connect the ADC digital interface pins. However, the disposition of the pins must still be considered. To wit:

DOUT: this pin is driven by the PCM3060, so we leave it floating.
LRCK1/BCK1: Both pins have an internal 50k pulldown, so we can safely leave these floating. However, we have a 1k resistor available because o f the I2C pins, so we use that to ground them both.
SCKI1: This is a floating (presumably hi-z) input, so we ground it to make sure we're not randomly clocking the ADC interface.

Because we're not using the analo g input functionality of the PCM3060, the VCOM pin is not used to bias any external circuitry. The bypass caps mounted here are to stabilize the value of this voltage, since it is used internally to the IC.

CDC.U.10

25 VIN L
26 VIN R
24 VCC
23 AGND1
16 SGND
22 AGND2
21 VCOM
20 VOUT L+
19 VOUT L-
18 VOUT R+
17 VOUT R-
13 ZEROR
14 ZEROL

7 VDD
8 DGND
3 DOUT
4 LRCK1
5 BCK1
6 SCKI1
12 DIN
11 LRCK2
10 BCK2
9 SCKI2
15 RST
28 MODE / MS/ADR/IFMD
27
1 MC/SCL/FMT
2 MD/SDA/DEMP

PCM3060

GND
4V6
3V3
CDC.C.36 0805 X5R 10uF 25V
CDC.C.37 0805 X5R 0.1uF 100V
CDC.C.38 0805 X5R 10uF 25V
CDC.C.39 0805 X5R 0.1uF 100V
CDC.C.25 0805 X5R 0.1uF 100V
CDC.C.35 0805 X5R 10uF 25V
CDC.Ra.1A 1206 Quad 1k 1%
CDC.Ra.1B 1206 Quad 1k 1%
CDC.Ra.1C 1206 Quad 1k 1%
CDC.Ra.1D 1206 Quad 1k 1%

PCM3060 VOUT L+
PCM3060 VOUT L-
PCM3060 VOUT R+
PCM3060 VOUT R-
PCM3060 DAC DIN
PCM3060 DAC LRCK
PCM3060 DAC BCK
PCM3060 DAC SCKI
PCM3060 RESET
PCM3060 SCL
PCM3060 SDA

The ZERO flags are outputs that indicat e to external things like mute circuits that there is nothing coming out on the DAC (lots of consecutive zeroes). This functionality doesn't really serve any purpose in this application, so we leave these pins floating since they're driven.

Connecting the MODE pin to DGND set s the PCM3060 to I2C mode. Connecting MODE to VDD would set it to SPI mode.

In I2C mode, the ADR pin sets the LSB o f the peripheral I2C address. In this case we ground it, so the peripheral address is b100 0110.

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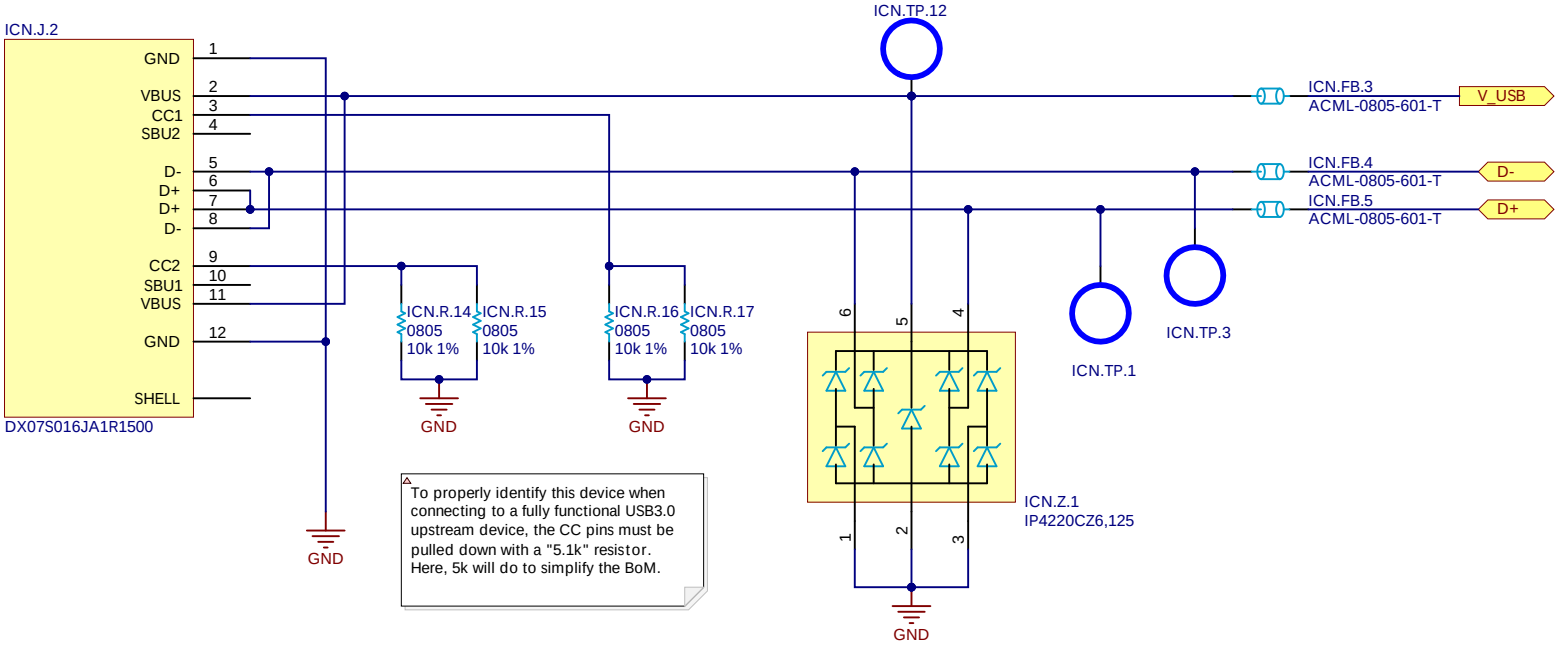

Title: InputConnectors.SchDoc		
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Pick and Place Fiducials

MCH.FID.1

IPC-7351 Fiducial 1mm

MCH.FID.2

IPC-7351 Fiducial 1mm

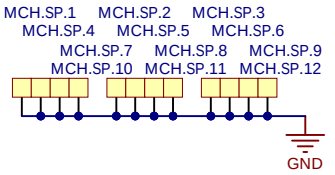
MCH.LOGO.1

Ploopy

Ploopy logo, silkscreen

Spark Gaps -- Case

Since the case has gaps in it, we expect ESD to worm its way in via creepage and perhaps other ways. To protect the board from this eventuality, we place spark gaps along the edges.



Title: Mechanical.SchDoc		
PCB: Gould.PrjPCB		Version: R1.007
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The SCKI nets have to be connected to one of the GPOUT<n> pins on the RP2040. These are GPIO21,23,24,25.

Only one of the two outputs has to actually send a clock over to the PCM3060, which can operate from one clock pin.

I2C pins are connected to every GPIO pin! SCL is connected to odd GPIO pin numbers and SDA is connected to even ones. Make sure you connect both pins to the SAME I2C port though (there are 2)!

PIO pins are mappable to all GPIO pins, so it doesn't matter where the I2S lines are hooked up.

Pins adjacent to I2S lines are grounded for signal integrity, since these signals go quite quickly. Unused pins are also grounded and should be set to output LOW to improve grounding.

This header can be pinched with tweezers or otherwise shorted during startup to force the RP2040 into USB bootloader mode. To do this, short the header while the board is unpowered, and then plug a USB cable in. If successful, the computer the RP2040 is attached to should detect a USB mass storage device that you can then drag and drop a new firmware file onto. Very cool!

MCU.J.4
HEADER2
MCU.R.9 0805 1k 1%
MCU.R.10 0805 10k 1%
3V3
GND

This flash chip holds all of the program memory. The chosen component is a 16MB chip, but smaller ones from the same series could be substituted in to reduce cost (there's about a CAD$1 difference to be had).

The nCS pin is tied high to ensure that the MCU normally boots off whatever is in flash. If you'd rather boot from USB, ground the nCS pin via the provided header and then reset the MCU using the RUN pin.

MCU.U.11
W25Q16JVSSIQ
CS, CLK, DI (IO0), DO (IO1), WP (IO2), HOLD or RESET (IO3), VCC, GND
MCU.C.40 0805 X5R 0.1uF 100V

This circuit translates the negative output voltage of the -9V inverting charge pump into a positive voltage that the MCU can read. Since the MCU outputs the PWM signal that controls the converter, reading this voltage allows for (in principle) closed loop control over the voltage if necessary, and a safety cut-off in case of overvoltage.

MCU.U.12
RP2040
GPIO0 PCM3060 SDA
GPIO1 PCM3060 SCL
GPIO2
GPIO3
GPIO4
GPIO5
GPIO6
GPIO7
GPIO8 PCM3060 DAC BCK
GPIO9 PCM3060 DAC LRCK
GPIO10
GPIO11
GPIO12 PCM3060 DAC DIN
GPIO13
GPIO14 PCM3060 RESET
GPIO15
GPIO16
GPIO17 INVERTING_SUPPLY_SWITCH
GPIO18
GPIO19 PCM3060 DAC SCKI
GPIO20
GPIO21
GPIO22 AUDIO_+SUPPLY_EN
GPIO23
GPIO24
GPIO25
GPIO26/ADC0
GPIO27/ADC1
GPIO28/ADC2
GPIO29/ADC3
QSPI_SS_N
QSPI_SCLK
QSPI_SD0
QSPI_SD1
QSPI_SD2
QSPI_SD3
USB_DP
USB_DM
USB_VDD
VREG_VIN
IO VDD
ADC_AVDD
XIN
XOUT
VREG_VOUT
D VDD
TESTEN
RUN
SW CLK
SWD IO
GND (PAD)

MCU.R.11 0805 22R 1% D+
MCU.R.12 0805 22R 1% D-

3V3
MCU.Ra.2A 1206 Quad 10k 1%
MCU.Ra.2B 1206 Quad 10k 1%
MCU.Ra.2C 1206 Quad 10k 1%
MCU.Ra.2D 1206 Quad 10k 1%
-9V
MCU.R.27 0805 100k 1%
GND

MCU.C.41 0805 X5R 1uF 25V
MCU.C.42 0805 X5R 0.1uF 100V
MCU.C.43 0805 X5R 0.1uF 100V
MCU.C.44 0805 X5R 0.1uF 100V
MCU.C.45 0805 X5R 0.1uF 100V
MCU.C.47 0805 X5R 0.1uF 100V
MCU.C.48 0805 X5R 0.1uF 100V

MCU.C.49 0603 18pF 50V
MCU.C.50 0603 18pF 50V
MCU.Y.1 RH100-12.000-16-3030 12MHz
MCU.R.13 0805 1k 1%

1V1
MCU.C.51 0805 X5R 1uF 25V
MCU.C.52 0805 X5R 0.1uF 100V
MCU.C.53 0805 X5R 0.1uF 100V

The digital core voltage is 1.1V, and it is generated by an on-chip linear regulator that outputs at VREG_VOUT.

The regulator requires a 1uF cap for stability at VREG_VIN and VREG_VOUT, and 0.1uF caps are added for each digital VDD pin for stability.

The RUN pin is the RP2040s external reset pin; pull it low to reset the part, using the provided header.

MCU.R.18 0805 1k 1%
MCU.TP.6
MCU.TP.5
MCU.TP.7

This header provides access to the SWD pins, just in case we need to do some hardcore debugging and/or have to rescue the chip.

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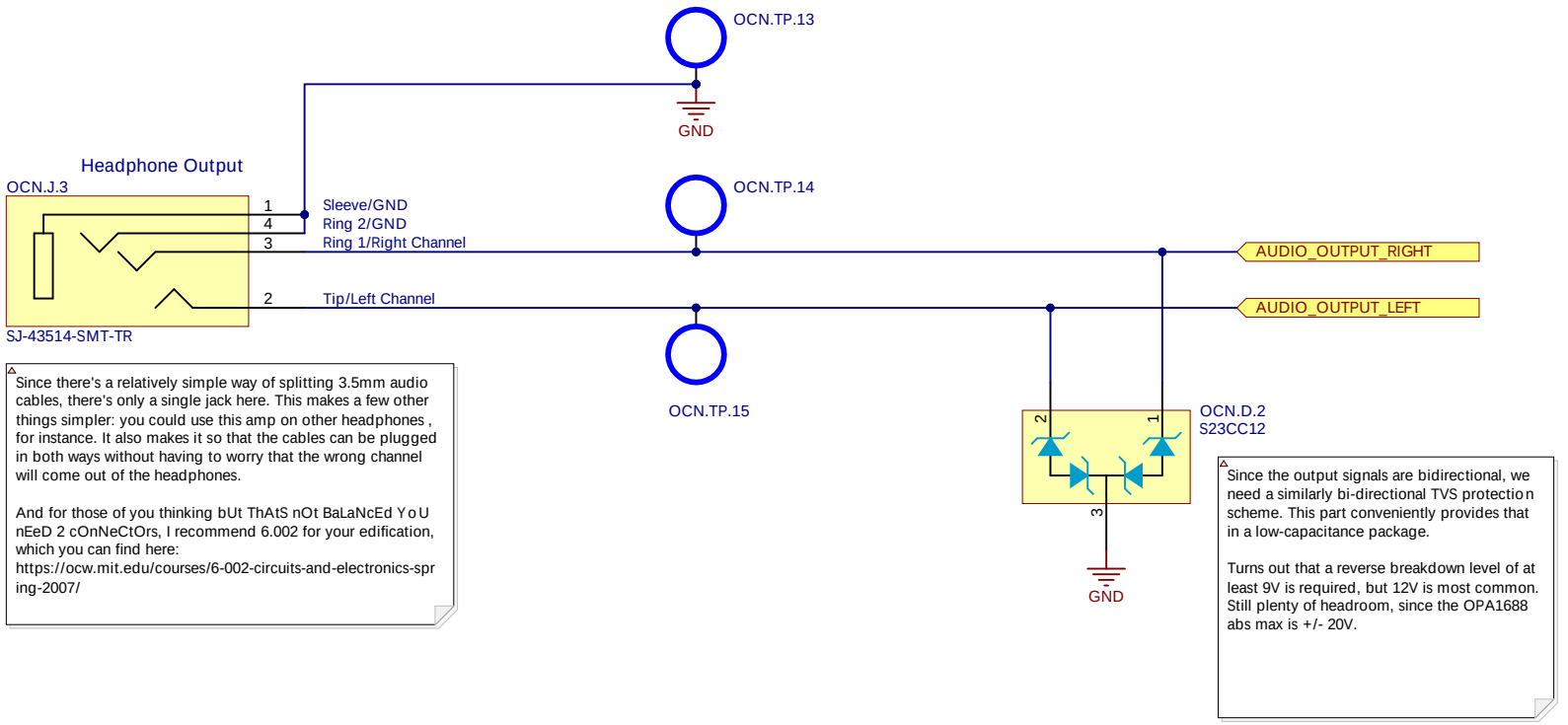

Title:	OutputConnectors.SchDoc		
PCB:	Gould.PrjPCB	Version:	R1.007
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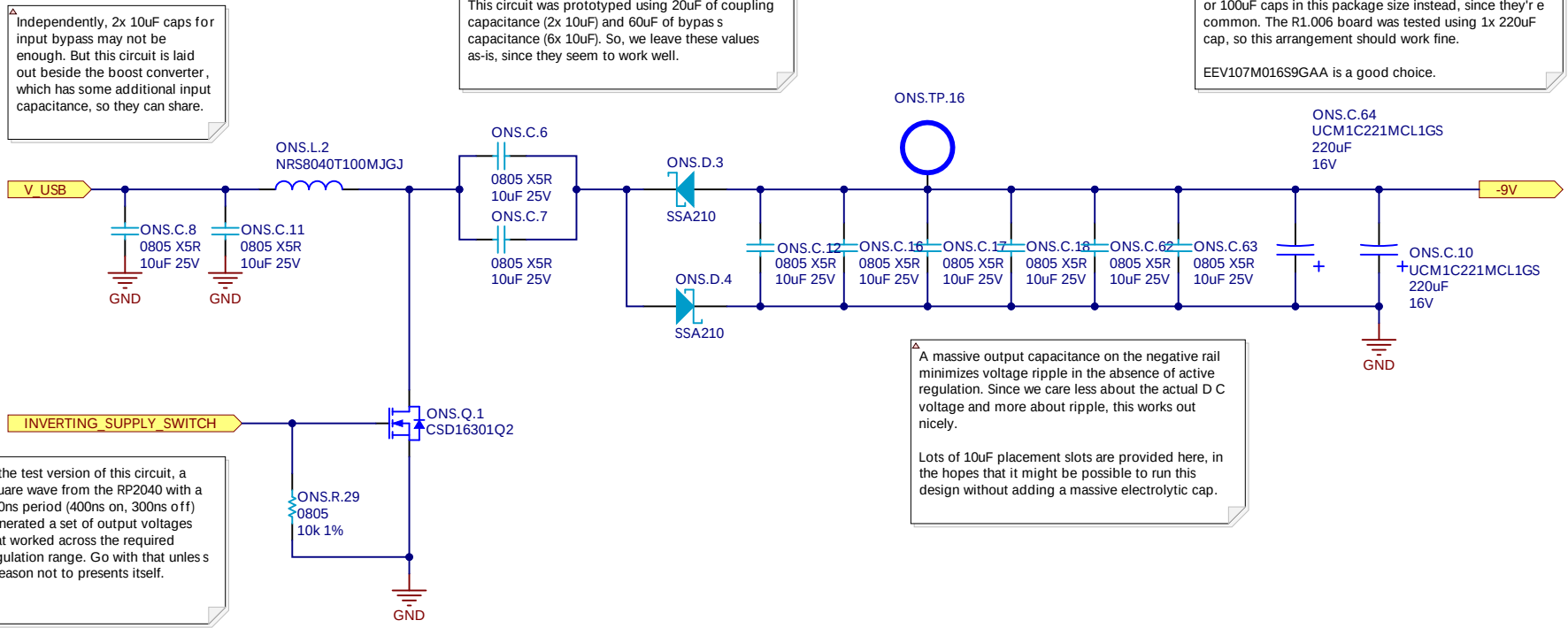

This circuit is pretty freaking weird. It's kind of an unregulated boost converter grafted onto a charge pump.

The FET/inductor combo produce a square-ish voltage that's some factor larger than V_USB when the FET is pulsed. The exact voltage is dependent on the timing of the FET activity, but is generally 2-5x V_USB. This waveform gets fed into an inverting charge pump, which turns it into a negative voltage that's somewhat less than the peak boost voltage.

Closed loop controllers for this topology are pretty hard to find, particularly right now (as of this writing, pretty much everything is hard to find reliably). So, we rely on two things: the op amps this circuit powers can run between -8V and -18V (a very large range) and they have a minimum PSRR of about -55dB. That means we can run this circuit pretty much unregulated as long as it produces between -18V and -8V between -35mA (the minimum quiescent current of the analog stages of the circuit) and -700mA (the maximum expected current draw at ear-splittingly loud volumes).

The good news is that it does. The even better news is that we could measure the output voltage on the RP2040 and either achieve closed-loop regulation or at the very least a safety shutdown if a negative overvoltage is detected. :D Details on how this works can be found in the source code running on the RP2040.

Title: OpAmpNegativeSupply.SchDoc			Ploopy Corporation
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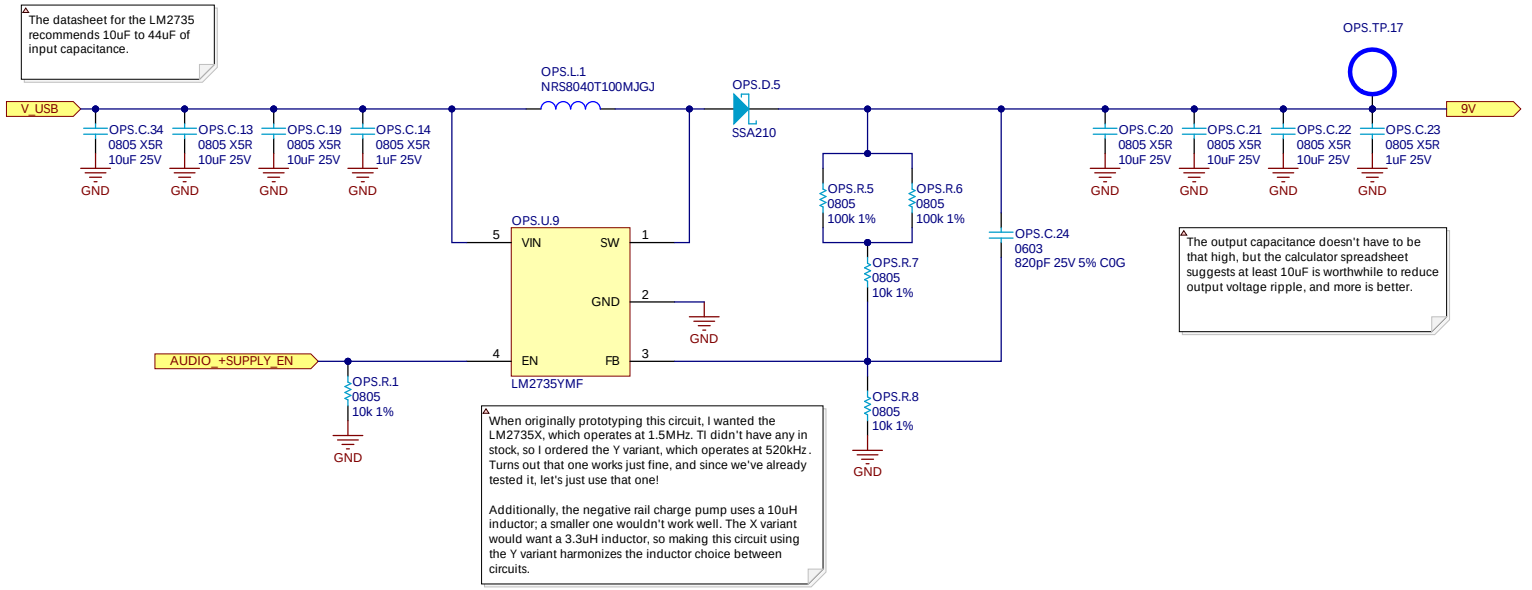

Title:	OpAmpSupply.SchDoc
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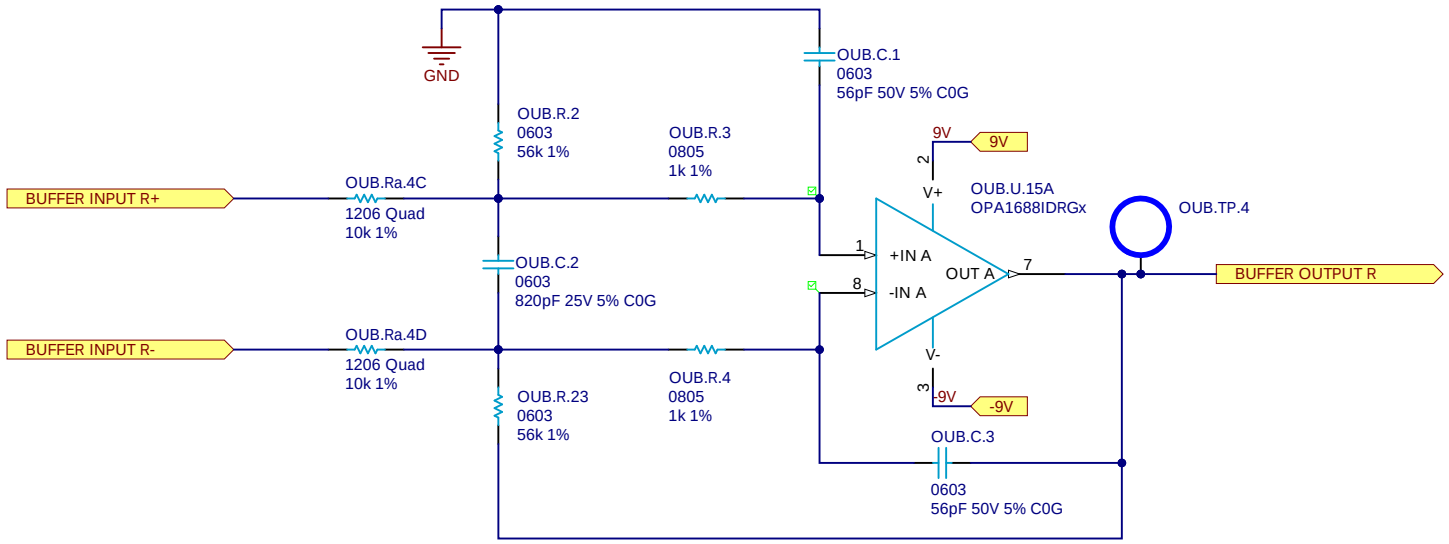
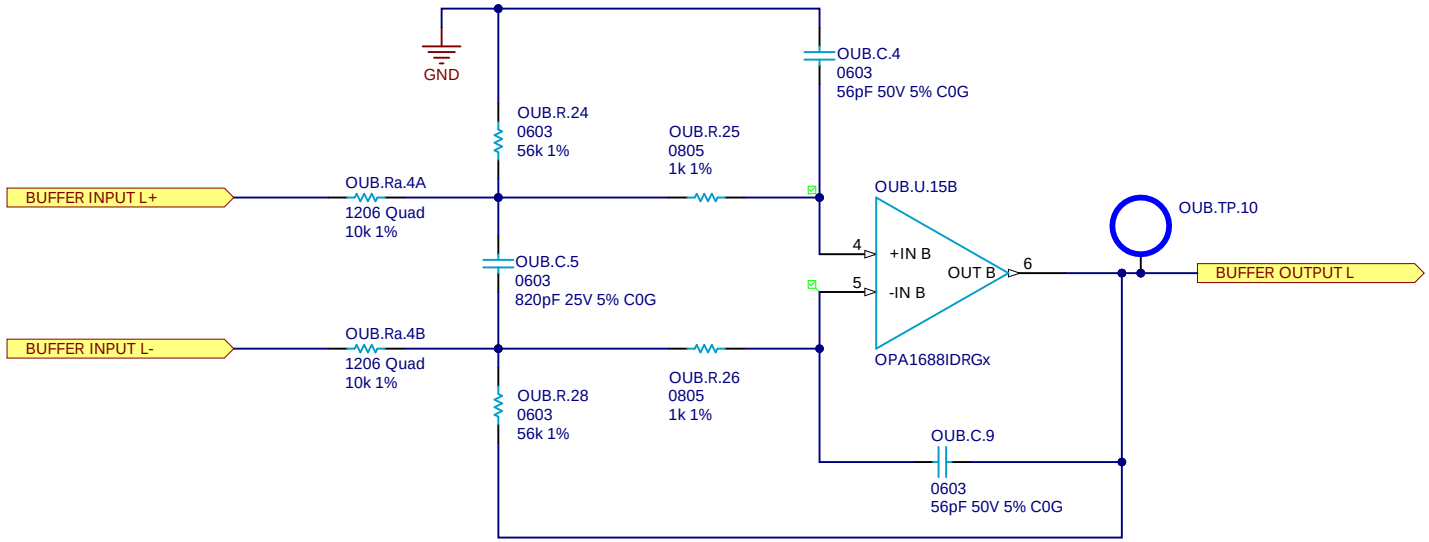
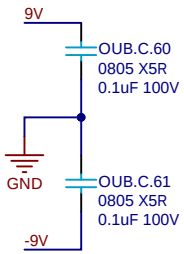
This sheet contains two op amps that provide signal gain/amplitude/differential and DC offset matching between the PCM3060 DAC and the power stage. The PCM3060 outputs a differential signal with a DC offset equal to 1/2 of its' analog supply voltage. This differential, offset signal must be converted to a single-ended signal with 0 offset to work with the power stage, which is what this circuit does.

Note the DC offset of 2.3V on the differential input voltage (from the DAC). However, at +/- 9V supply voltage, the 2.3V DC offset is in no danger of upsetting the apple cart (the allowable max Vcm is V+ - 2V, or 7V), so there's no worries to be had.

The original design comes from the PCM3060 datasheet (page 40, Fig. 34(b)), and appears to be a differential MFA topology. Analysis is complicated, so simulations were done to optimize the frequency response. Interestingly, this topology is quite sensitive to changes in component values, so passive tolerances should be minimized where practical. 5% caps have been specified for this purpose.







Title: OutputBuffer.SchDoc			
PCB: Gould.PrjPCB		Version: R1.007	
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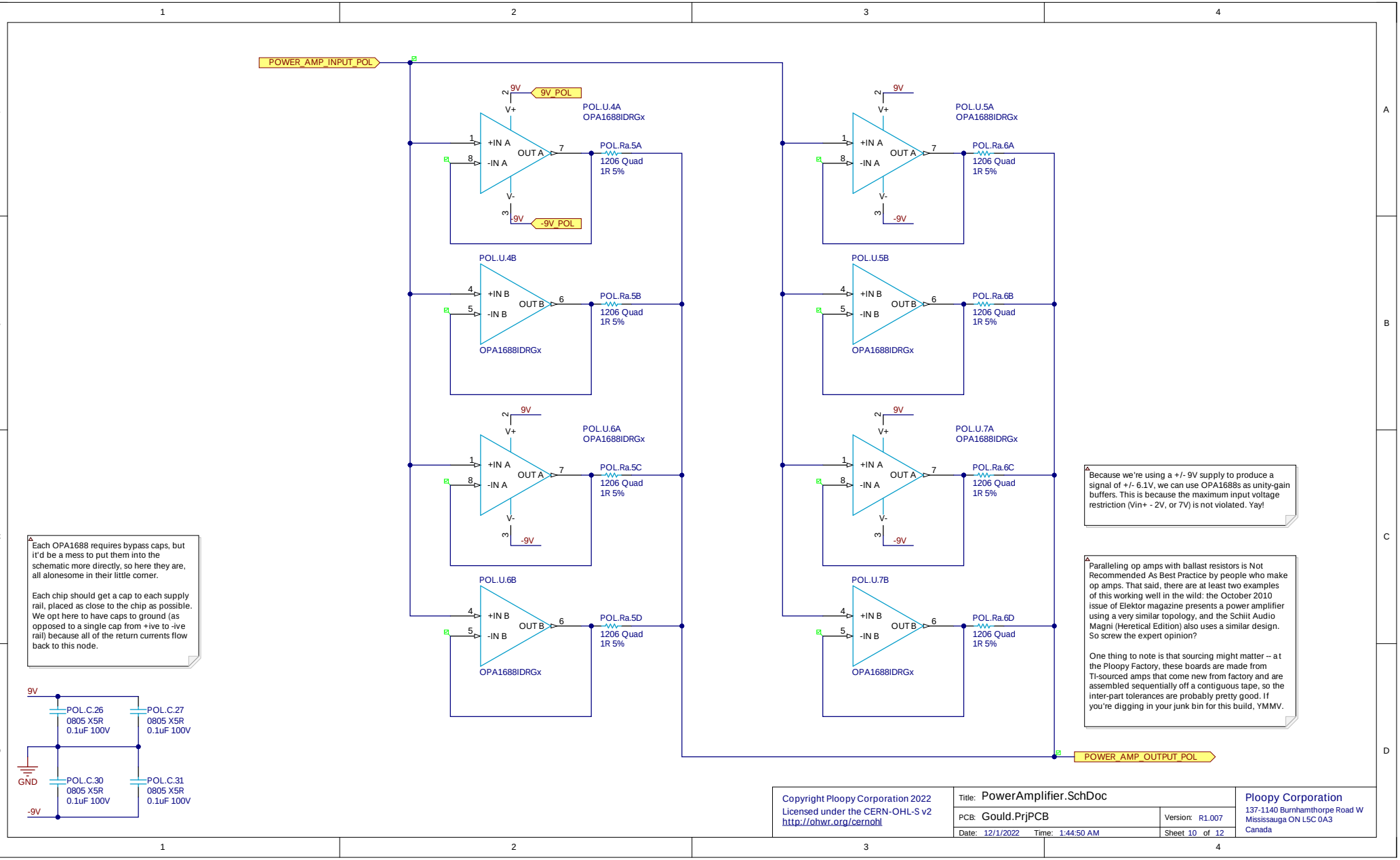

Title:	PowerAmplifier.SchDoc
PCB:	Gould.PrjPCB
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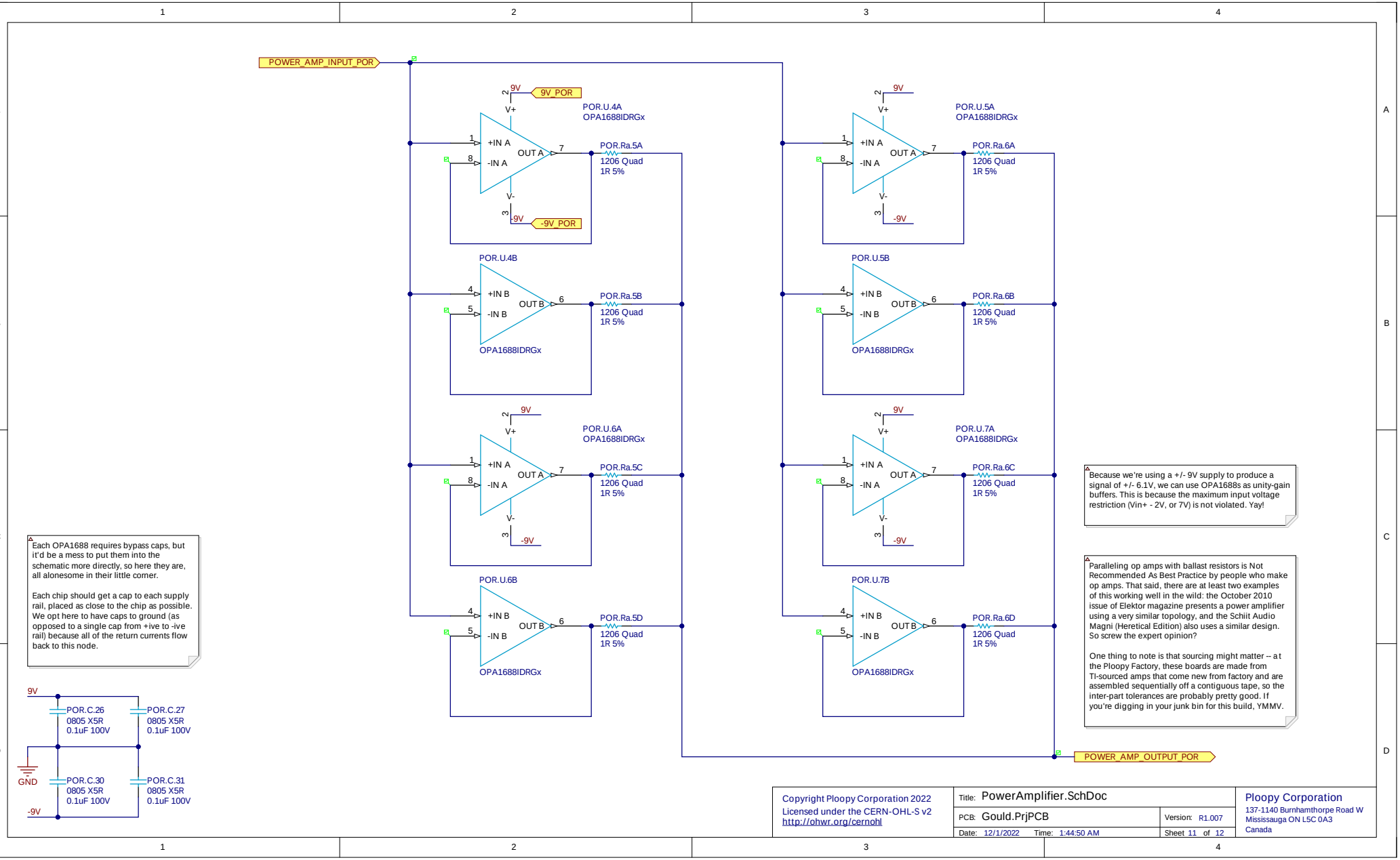

Title:	PowerAmplifier.SchDoc
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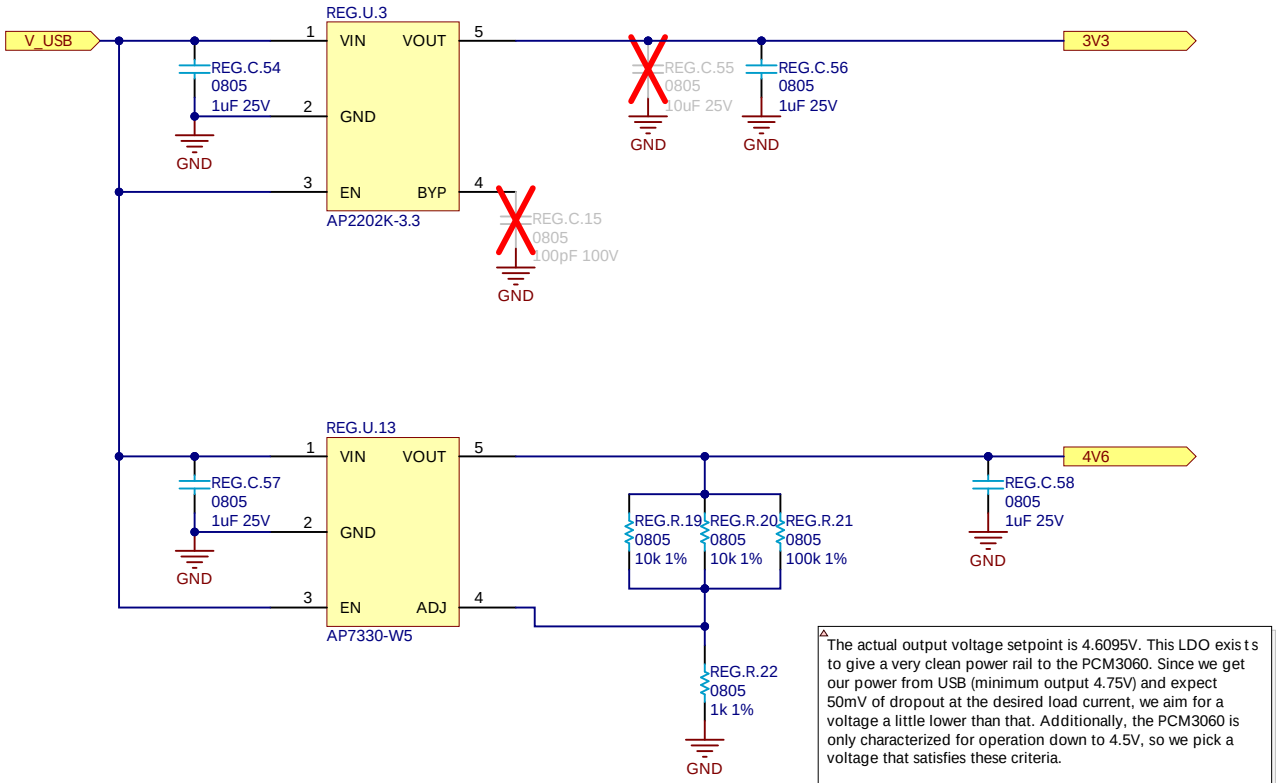

Title: Regulators.SchDoc			
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